REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-28 in the application. In previous responses, the Applicant added Claim 29 and subsequently canceled Claims 23-29 without prejudice or disclaimer. In the present response, the Applicant has amended independent Claims 1 and 22 to further clarify previously presented limitations. Claims 1 and 22 have also been amended in response to pending Claims Objections and 35 U.S.C. §101 rejection. Additionally, the Applicant has added independent Claim 30 which combines the limitations of presently amended independent Claim 1 and previously presented dependent Claim 16. No other claims have been added or canceled. Accordingly, Claims 1-22 and 30 are currently pending in the application.

II. Formal Matters and Objections

The Examiner has objected to Claims 1 and 22 as containing informalities. As noted above, the Applicant has amended these claims according to the Examiner's suggestions at items 2-3 on page 2 of the Office Action. With regard to the claim language in Claim 22 where a plurality of instructions are decoded to detect whether a data processing instruction defines a fixed or configurable instruction, the Applicant confirms that the invention is consistent with this claim language. That is, a plurality of instructions is decoded to detect whether at least one of data processing instructions of the plurality of instructions defines a fixed data processing instruction or a configurable data processing instruction. Accordingly, the Applicant respectfully requests the Examiner to withdraw the objection to Claims 1 and 22 and allow issuance thereof.

II. Rejection of Claims 1-21 under 35 U.S.C. §101

The Examiner has rejected Claims 1-21 under 35 U.S.C. §101 because Claims 1-21 are directed to software, per se. As noted above, the Applicant has amended Claim 1 according to the Examiner's suggestions so that Claim 1 now complies with the requirements of 35 U.S.C. §101. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §101 rejection of Claims 1-21 and allow issuance thereof.

II. Rejection of Claims 1-22 under 35 U.S.C. §103

The Examiner has rejected Claims 1-22 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,737,631 to Trimberger (hereinafter "Trimberger") in view of an article entitled "Configurable Multiplier Blocks for use within an FPGA", 1998 by Haynes, *et al.* (hereinafter "Haynes"), and further in view of an article entitled "A Flexible LUT-Based Carry Chain for FPGAs", 2003 by Lodi, *et al.* (hereinafter "Lodi") and in further view of U.S. Patent No. 7,176,713 to Madurawe (hereinafter "Madurawe"). The Applicant respectfully disagrees in view of the amendment.

At item 8b at the top of page 4 of the Office Action, the Examiner alleges that Trimberger discloses a dedicated control processing facility having its own control register file, pointing to execution unit 100 and register file 103, 140. As noted above, independent Claims 1 and 22 have been amended to more clearly point out that the control execution path of the dedicated control processing facility is dedicated to processing control instructions and also that the dedicated control processing facility comprises functional units. Trimberger only has a single execution unit 100.

Furthermore, execution unit 100 and its registers 140 are not dedicated to the processing of control instructions. As stated in line 65 of column 5 of Trimberger, the execution unit provides a general purpose microprocessor. That is, this execution unit handles all instructions in the program, apart from the instructions which will be handled by RISA 21.

Additionally, Claim 1 has been amended, as noted above, to more clearly point out that the decode unit is operable to separate control instructions from data processing instructions. At item 8d on page 5 of the Office Action, the Examiner addresses this. The decoder 112 in Trimberger does not separate different classes of instructions. Instead, it supplies the opcode from the instructions to the instruction input I on the defined execution unit 100 and to the instruction port I on the RISA FPGA 120. It is clear that the decoder 112 does not separate the instructions into different classes. In fact, in Trimberger, there is an instruction format in which a defined instruction opcode field and a programmed instruction opcode field are present in the same instruction where these opcodes are simultaneously applied to the execution unit 100 and the RISA FPGA 120. (*See, e.g.*, Fig. 5 and lines 41-57 of column 9 of Trimberger.) There is clearly no separation of the instructions for supply to separate dedicated processing paths as recited in presently amended independent Claims 1 and 22.

Furthermore Claims 1 and 22 have been amended to more clearly point out that the decode unit is operable to supply a control instruction to one of the functional units. As noted above, Trimberger teaches only a single execution unit 100 and not multiple functional units to one of which a control instruction is supplied. It is further noted that in Trimberger, the decoder provides common signals to the remainder of the processing path as denoted by arrows 113 in Fig. 2. There is

no attempt to separate different classes of instructions at the decoder nor are there separate dedicated control and data processing facilities in Trimberger to handle these instructions.

At item 8d at the top of page 5 of the Office Action, the Examiner suggests that Trimberger discloses a dedicated data processing facility, citing component 120. As noted above, independent Claims 1 and 22 have been amended to more clearly point out that the dedicated data processing facility is dedicated to processing data processing instructions. This now makes it clear that the data processing facility is dedicated to processing data processing instructions which are separated from the control instructions by the decode unit. As established above, the decode unit of Trimberger does not implement this separating function and, thus, Trimberger does not disclose such a dedicated data processing facility. It is further noted that the component 120 of Trimberger does not execute all the data processing instructions, but only instructions appropriate to the configuration of the FPGA.

At item 8d at the middle of page 4 of the Office Action, the Examiner recognizes that Trimberger does not disclose that the data processing facility comprises a first data execution path and a second data execution path but cites that there is some combination of Haynes, Lodi, and Madurawe which would result in such a configuration. There is no basis on which a person of ordinary skill in the art at the time of the invention, without the benefit of the teachings of the present invention, could derive such a combination of these documents without improper hindsight.

The Examiner, at item 8e at the top of page 6 of the Office Action, acknowledges that Trimberger does not teach that the dedicated control processing facility includes a branch unit and a load/store unit but that it would have been obvious to incorporate these because of the condition codes referred to by Trimberger. In Trimberger, however, these condition codes are utilized by an

instruction control state machine 107 which manages the instruction sequencing decisions. (*See, e.g.*, lines 35-38 of column 7 of Trimberger.) It appears these instruction sequencing decisions are handled for the whole system and, therefore, there is no motivation in Trimberger to include a separate branch unit which is dedicated just to the execution unit 100 (equated as the claimed dedicated control processing facility).

Also at item 8e at the middle of page 6 of the Office Action, the Examiner acknowledges that Trimberger does not teach that the dedicated control processing facility includes a load/store unit. Loading and storing is accomplished in Trimberger using external ports connected to external memory as shown on the right and left hand sides of Fig. 2. There would be no need to include a separate load/store unit dedicated only to the execution unit 100 because the ports in Trimberger perform the necessary task of loading and storing to and from external memory for all of the units in the system.

At item 8f at the bottom of page 6 of the Office Action, the Examiner suggests that Trimberger teaches that the controller is operable to configure the connectivity of the configurable operators in accordance with configuration information provided in an opcode portion of a configurable data processing instruction, citing lines 31-33 of column 3 of Trimberger. This part of Trimberger suggests that the RISA can be reprogrammed by a program. That is, instructions can be provided which reprogram the RISA. However, Trimberger does not disclose that the data processing instructions themselves include the configuration information in their opcode portion. The opcode portions of the instructions of Trimberger are shown in Figs. 3-5 and emphatically do not contain any configuration information.

Configuration of the RISA is done as a separate matter, as discussed in lines 39-44 of column 8 of Trimberger. While the RISA is being configured, it cannot be used to execute instructions. Thus, Trimberger cannot and does not disclose data processing instructions which are supplied to the data execution path for processing and which include configuration information in their opcode portion.

Furthermore, the Examiner suggests that Trimberger teaches the supply of a fixed path instruction to "fixed FPGA circuitry" and a configurable instruction to "configurable FPGA circuitry." There is no disclosure in Trimberger of "fixed FPGA circuitry." The entire FPGA 120 of Trimberger is configurable.

For at least the reasons given above, the cited portions of the cited combination of Trimberger, Haynes, Lodi, and Madurawe, as applied by the Examiner do not provide a *prima facie* case of obviousness for presently amended independent Claims 1 and 22 and newly presently independent Claim 30 and Claims that depend thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §103(a) rejection of Claims 1-22 and allow issuance of the pending claims.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-22 and 30.

The Applicant requests the Examiner to telephone the undersigned agent of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

HITT GAINES, PC

/Steven J. Hanke

Steven J. Hanke
Registration No. 58,076

Dated: June 10, 2010

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800